National Semiconductor

July 2005

LMH6622
Dual Wideband, Low Noise, 160MHz, Operational Amplifiers

General Description

The LMH6622 is a dual high speed voltage feedback operational amplifier specifically optimized for low noise. A voltage noise specification of 1.6nV/$\sqrt{Hz}$, a current noise specification 1.5pA/$\sqrt{Hz}$, a bandwidth of 160MHz, and a harmonic distortion specification that exceeds 90dBc combine to make the LMH6622 an ideal choice for the receive channel amplifier in ADSL, VDSL, or other xDSL designs. The LMH6622 operates from ±2.5V to ±6V in dual supply mode and from +5V to +12V in single supply configuration. The LMH6622 is stable for $A_V \geq 2$ or $A_V \leq -1$. The fabrication of the LMH6622 on National Semiconductor's advanced VIP10 process enables excellent (160MHz) bandwidth at a current consumption of only 4.3mA/amplifier. Packages for this dual amplifier are the 8-lead SOIC and the 8-lead MSOP.

Features

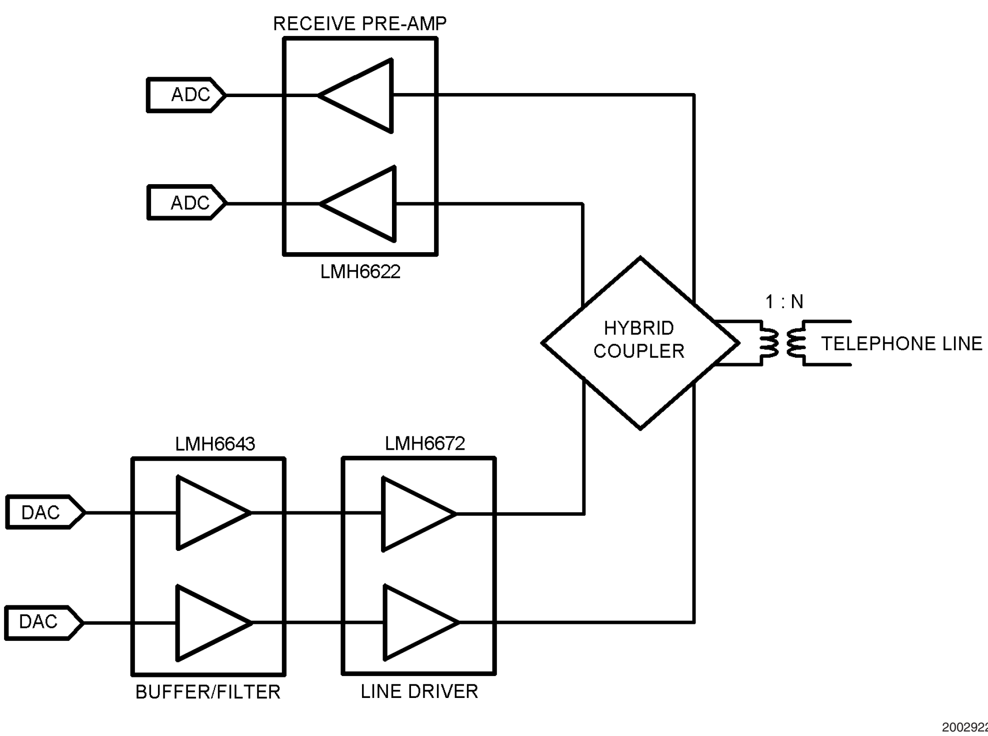
V_S = ±6V, T_A = 25˚C, Typical values unless specified

- Bandwidth (A_V = +2) 160MHz
- Supply Voltage Range ±2.5V to ±6V +5V to +12
- Slew rate 85V/µs
- Supply current 4.3mA/amp
- Input common mode voltage −4.75V to +5.7V
- Output Voltage Swing (R_L = 100Ω) ±4.6V
- Input voltage noise 1.6nV/$\sqrt{Hz}$
- Input current noise 1.5pA/$\sqrt{Hz}$
- Linear output current 90mA
- Excellent harmonic distortion 90dBc

Applications

- xDSL receiver
- Low noise instrumentation front end
- Ultrasound preamp
- Active filters
- Cellphone basestation

xDSL Analog Front End



LMH6622 Dual Wideband, Low Noise, 160MHz, Operational Amplifiers

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance	
Human Body Model	2kV (Note 2)
Machine Model	200V (Note 2)
V_{IN} Differential	±1.2V
Supply Voltage ($V^+ - V^-$)	13.2V
Voltage at Input Pins	V^+ +0.5V, V^- −0.5V
Soldering Information	
Infrared or Convection (20 sec)	235˚C
Wave Soldering (10 sec)	260˚C
Storage Temperature Range	−65˚C to +150˚C
Junction Temperature (Note 4)	+150˚C

Operating Ratings (Note 1)

Supply Voltage ($V^+ - V^-$)	±2.25V to ±6V
Junction Temperature Range (Note 3), (Note 4)	−40˚C to +85˚C
Package Thermal Resistance (Note 4) (θ_{JA})	
8-pin SOIC	166˚C/W
8-pin MSOP	211˚C/W

±6V Electrical Characteristics

Unless otherwise specified, T_J = 25˚C, V^+ = 6V, V^- = −6V, V_{CM} = 0V, A_V = +2, R_F = 500Ω, R_L = 100Ω. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
Dynamic Performance						
f_{CL}	−3dB BW	V_O = 200mV_{PP}		160		MHz
$BW_{0.1dB}$	0.1dB Gain Flatness	V_O = 200mV_{PP}		30		MHz
SR	Slew Rate (Note 8)	V_O = 2V_{PP}		85		V/µs
TS	Settling Time	V_O = 2V_{PP} to ±0.1%		40		ns
		V_O = 2V_{PP} to ±1.0%		35		
Tr	Rise Time	V_O = 0.2V Step, 10% to 90%		2.3		ns
Tf	Fall Time	V_O = 0.2V Step, 10% to 90%		2.3		ns
Distortion and Noise Response						
e_n	Input Referred Voltage Noise	f = 100kHz		1.6		$nV/\sqrt{Hz}$
i_n	Input Referred Current Noise	f = 100kHz		1.5		$pA/\sqrt{Hz}$
DG	Differential Gain	R_L = 150Ω, R_F = 470Ω, NTSC		0.03		%
DP	Differential Phase	R_L = 150Ω, R_F = 470Ω, NTSC		0.03		deg
HD2	2nd Harmonic Distortion	f_c = 1MHz, V_O = 2V_{PP}, R_L = 100Ω		−90		dBc
		f_c = 1MHz, V_O = 2V_{PP}, R_L = 500Ω		−100		
HD3	3rd Harmonic Distortion	f_c = 1MHz, V_O = 2V_{PP}, R_L = 100Ω		−94		dBc
		f_c = 1MHz, V_O = 2V_{PP}, R_L = 500Ω		−100		
MTPR	Upstream	V_O = 0.6 V_{RMS}, 26kHz to 132kHz (see test circuit 5)		−78		dBc
	Downstream	V_O = 0.6 V_{RMS}, 144kHz to 1.1MHz (see test circuit 5)		−70		
Input Characteristics						
V_{OS}	Input Offset Voltage	V_{CM} = 0V	−1.2 **−2**	+0.2	+1.2 **+2**	mV
TC V_{OS}	Input Offset Average Drift	V_{CM} = 0V (Note 7)		−2.5		µV/˚C
I_{OS}	Input Offset Current	V_{CM} = 0V	−1 **−1.5**	−0.04	1 **1.5**	µA
I_B	Input Bias Current	V_{CM} = 0V		4.7	10 **15**	µA
R_{IN}	Input Resistance	Common Mode		17		MΩ
		Differential Mode		12		kΩ
C_{IN}	Input Capacitance	Common Mode		0.9		pF
		Differential Mode		1.0		pF

±6V Electrical Characteristics (Continued)

Unless otherwise specified, $T_J = 25^{\circ}C$, $V^+ = 6V$, $V^- = -6V$, $V_{CM} = 0V$, $A_V = +2$, $R_F = 500\Omega$, $R_L = 100\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
CMVR	Input Common Mode Voltage Range	CMRR ≥ 60dB		−4.75	−4.5	V
			5.5	+5.7		
CMRR	Common-Mode Rejection Ratio	Input Referred, $V_{CM} = -4.2$ to $+5.2V$	80 **75**	100		dB
Transfer Characteristics						
A_{VOL}	Large Signal Voltage Gain	$V_O = 4V_{PP}$	74 **70**	83		dB
X_t	Crosstalk	f = 1MHz		−75		dB
Output Characteristics						
V_O	Output Swing	No Load, Positive Swing	4.8 **4.6**	5.2		V
		No Load, Negative Swing		−5.0	−4.6 **−4.4**	
		$R_L = 100\Omega$, Positive Swing	4.0 **3.8**	4.6		
		$R_L = 100\Omega$, Negative Swing		−4.6	−4 **−3.8**	
R_O	Output Impedance	f = 1MHz		0.08		Ω
I_{SC}	Output Short Circuit Current	Sourcing to Ground $\Delta V_{IN} = 200mV$ (Note 3), (Note 9)	100	135		mA
		Sinking to Ground $\Delta V_{IN} = -200mV$ (Note 3), (Note 9)	100	130		
I_{OUT}	Output Current	Sourcing, $V_O = +4.3V$ Sinking, $V_O = -4.3V$		90		mA
Power Supply						
+PSRR	Positive Power Supply Rejection Ratio	Input Referred, $V_S = +5V$ to $+6V$	80 **74**	95		dB
−PSRR	Negative Power Supply Rejection Ratio	Input Referred, $V_S = -5V$ to $-6V$	75 **69**	90		
I_S	Supply Current (per amplifier)	No Load		4.3	6 **6.5**	mA

±2.5V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^{\circ}C$, $V^+ = 2.5V$, $V^- = -2.5V$, $V_{CM} = 0V$, $A_V = +2$, $R_F = 500\Omega$, $R_L = 100\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
Dynamic Performance						
f_{CL}	−3dB BW	$V_O = 200mV_{PP}$		150		MHz
$BW_{0.1dB}$	0.1dB Gain Flatness	$V_O = 200mV_{PP}$		20		MHz
SR	Slew Rate (Note 8)	$V_O = 2V_{PP}$		80		V/μs
T_S	Settling Time	$V_O = 2V_{PP}$ to ±0.1%		45		ns
		$V_O = 2V_{PP}$ to ±1.0%		40		
T_r	Rise Time	$V_O = 0.2V$ Step, 10% to 90%		2.5		ns
T_f	Fall Time	$V_O = 0.2V$ Step, 10% to 90%		2.5		ns
Distortion and Noise Response						
e_n	Input Referred Voltage Noise	f = 100kHz		1.7		$nV/\sqrt{Hz}$
i_n	Input Referred Current Noise	f = 100kHz		1.5		$pA/\sqrt{Hz}$

±2.5V Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = 2.5V, V^- = –2.5V, V_{CM} = 0V, A_V = +2, R_F = 500Ω, R_L = 100Ω. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
HD2	2nd Harmonic Distortion	fc = 1MHz, V_O = 2V_{PP}, R_L = 100Ω		–88		dBc
		fc = 1MHz, V_O = 2V_{PP}, R_L = 500Ω		–98		
HD3	3rd Harmonic Distortion	fc = 1MHz, V_O = 2V_{PP}, R_L = 100Ω		–92		dBc
		fc = 1MHz, V_O = 2V_{PP}, R_L = 500Ω		–100		
MTPR	Upstream	V_O = 0.4V_{RMS},26kHz to 132kHz (see test circuit 5)		–76		dBc
	Downstream	V_O = 0.4V_{RMS},144kHz to 1.1MHz (see test circuit 5)		–68		
Input Characteristics						
V_{OS}	Input Offset Voltage	V_{CM} = 0V	–1.5 **–2.3**	+0.3	+1.5 **+2.3**	mV
TC V_{OS}	Input Offset Average Drift	V_{CM} = 0V (Note 7)		–2.5		µV/˚C
I_{OS}	Input Offset Current	V_{CM} = 0V	–1.5 **–2.5**	+0.01	1.5 **2.5**	µA
I_B	Input Bias Current	V_{CM} = 0V		4.6	10 **15**	µA
R_{IN}	Input Resistance	Common Mode		17		MΩ
		Differential Mode		12		kΩ
C_{IN}	Input Capacitance	Common Mode		0.9		pF
		Differential Mode		1.0		pF
CMVR	Input Common Mode Voltage Range	CMRR ≥ 60dB		–1.25	–1	V
			2	+2.2		
CMRR	Common Mode Rejection Ratio	Input Referred, V_{CM} = –0.7 to +1.7V	80 **75**	100		dB
Transfer Characteristics						
A_{VOL}	Large Signal Voltage Gain	V_O = 1V_{PP}	74	82		dB
X_t	Crosstalk	f = 1MHz		–75		dB
Output Characteristics						
V_O	Output Swing	No Load, Positive Swing	1.4 **1.2**	1.7		V
		No Load, Negative Swing		–1.5	–1.2 **–1**	
		R_L = 100Ω, Positive Swing	1.2 **1**	1.5		
		R_L = 100Ω, Negative Swing		–1.4	–1.1 **–0.9**	
R_O	Output Impedance	f = 1MHz		0.1		Ω
I_{SC}	Output Short Circuit Current	Sourcing to Ground ΔV_{IN} = 200mV (Note 3), (Note 9)	100	137		mA
		Sinking to Ground ΔV_{IN} = –200mV (Note 3), (Note 9)	100	134		
I_{OUT}	Output Current	Sourcing, V_O = +0.8V Sinking, V_O = –0.8V		90		mA
Power Supply						
+PSRR	Positive Power Supply Rejection Ratio	Input Referred, V_S = +2.5V to +3V	78 **72**	93		dB
–PSRR	Negative Power Supply Rejection Ratio	Input Referred, V_S = –2.5V to –3V	75 **70**	88		dB

±2.5V Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = 2.5V, V^- = −2.5V, V_{CM} = 0V, A_V = +2, R_F = 500Ω, R_L = 100Ω. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
I_S	Supply Current (per amplifier)	No Load		4.1	5.8 **6.4**	mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5kΩ in series with 100pF. Machine model, 0Ω in series with 200pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150˚C.

Note 4: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = $(T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

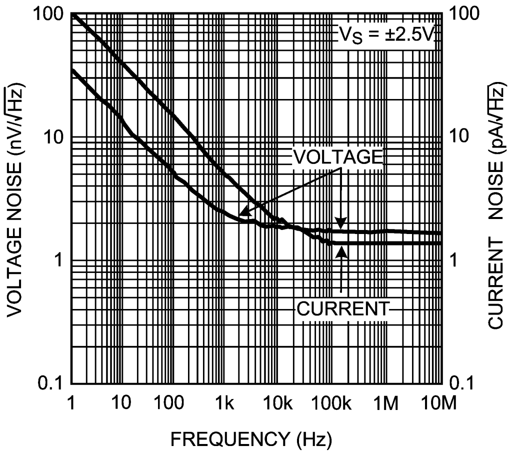
Note 7: Offset voltage average drift is determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

Note 8: Slew rate is the slowest of the rising and falling slew rates.

Note 9: Short circuit test is a momentary test. Output short circuit duration is infinite for $V_S \leq \pm 2.5V$, at room temperature and below. For $V_S > \pm 2.5V$, allowable short circuit duration is 1.5ms.

Typical Performance Characteristics

Current and Voltage Noise vs. Frequency



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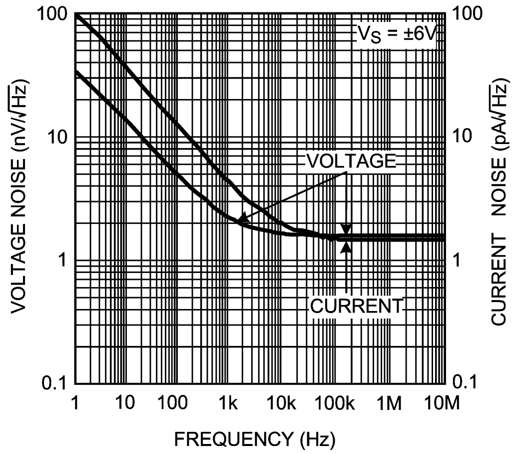
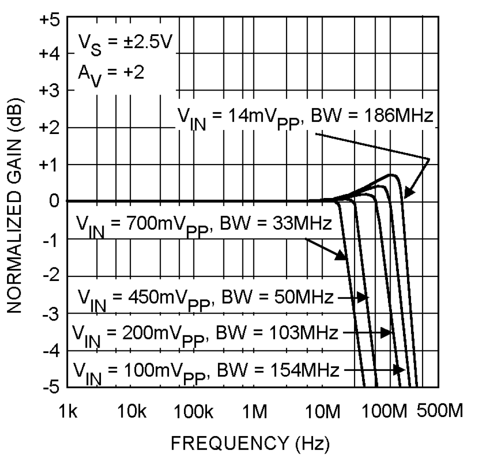
Current and Voltage Noise vs. Frequency



20029225

Frequency Response vs. Input Signal Level



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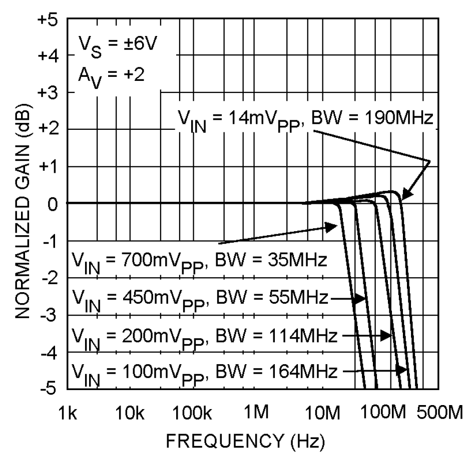
Frequency Response vs. Input Signal Level



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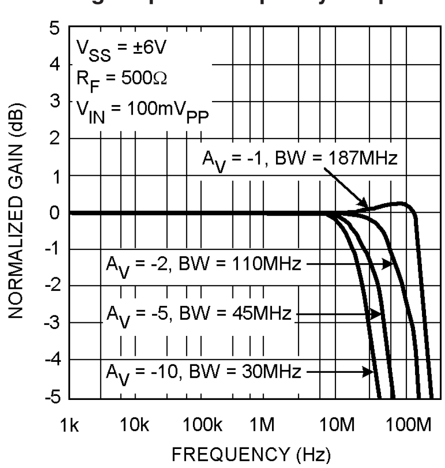
Inverting Amplifier Frequency Response



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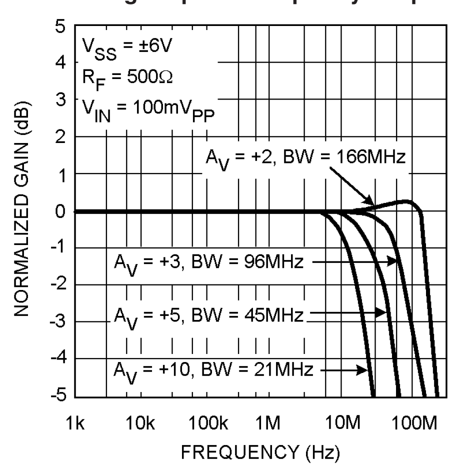
Non-Inverting Amplifier Frequency Response



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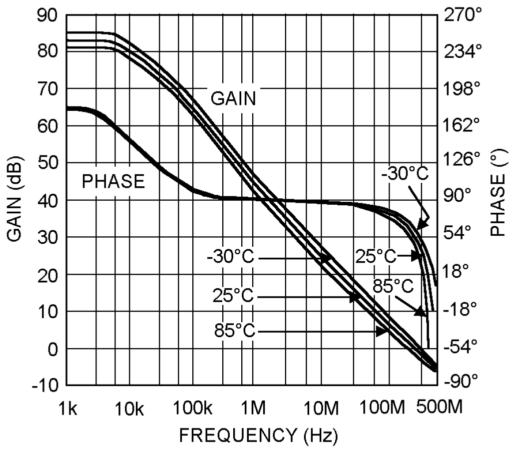
Typical Performance Characteristics (Continued)

Open Loop Gain and Phase Response



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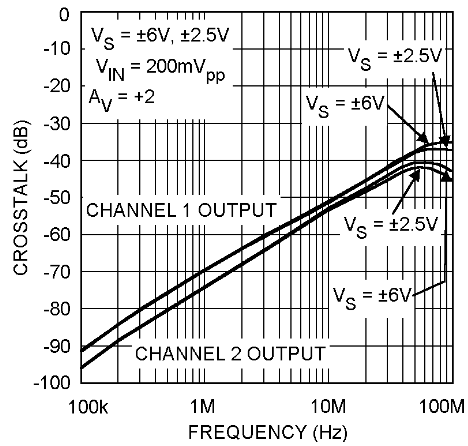
Crosstalk vs. Frequency



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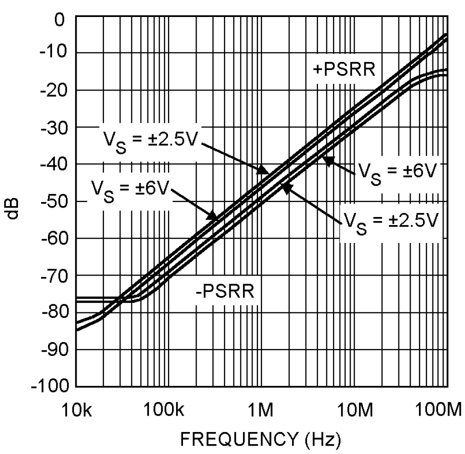
PSRR vs. Frequency



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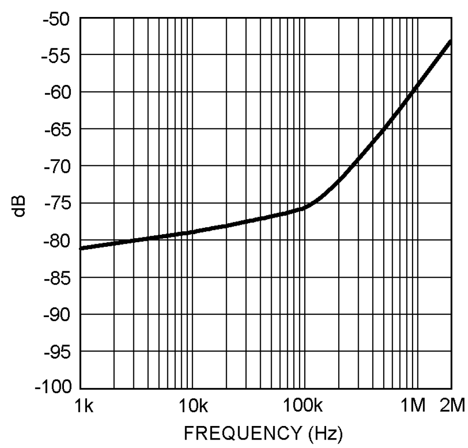
CMRR vs. Frequency



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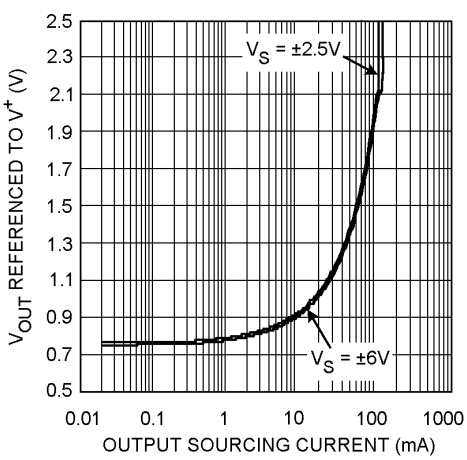
Positive Output Swing vs. Source Current



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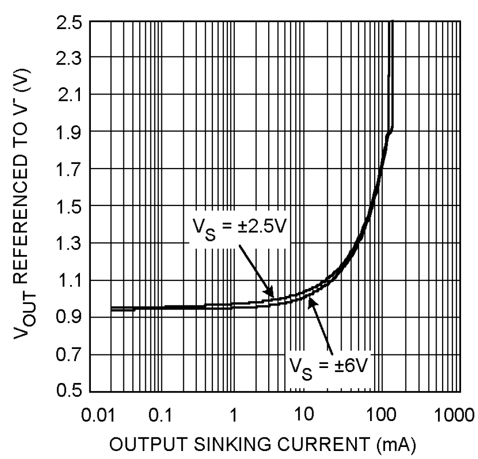
Negative Output Swing vs. Sink Current



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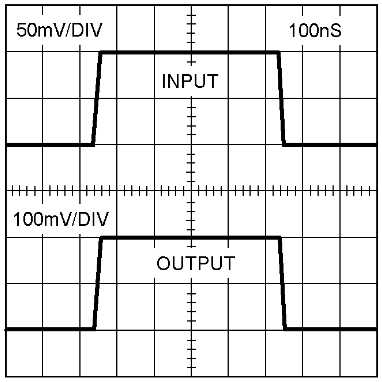
Typical Performance Characteristics (Continued)

Non-Inverting Small Signal Pulse Response
V_S = ±2.5V, R_L = 100Ω, A_V = +2, R_F = 500Ω



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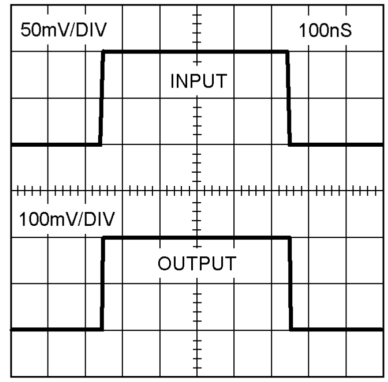
Non-Inverting Small Signal Pulse Response
V_S = ±6V, R_L = 100Ω, A_V = +2, R_F = 500Ω



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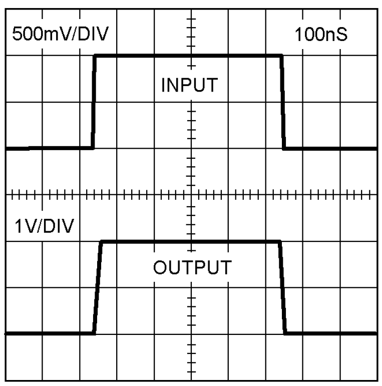
Non-Inverting Large Signal Pulse Response
V_S = ±2.5V, R_L = 100Ω, A_V = +2, R_F = 500Ω



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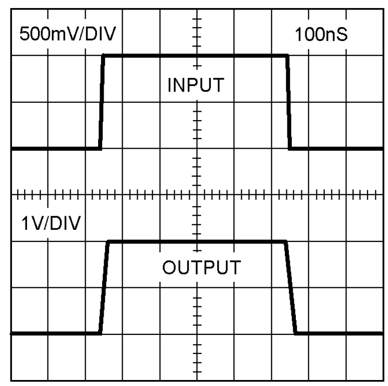
Non-Inverting Large Signal Pulse Response
V_S = ±6V, R_L = 100Ω, A_V = +2, R_F = 500Ω



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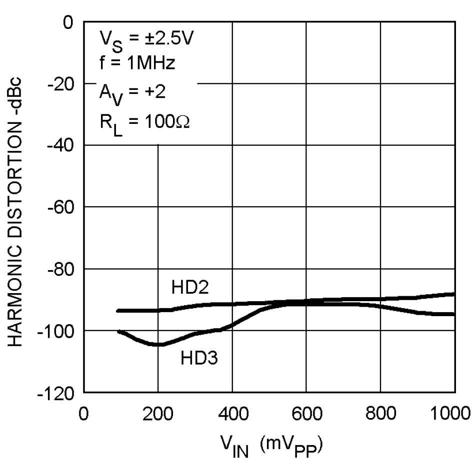
Harmonic Distortion vs. Input Signal Level



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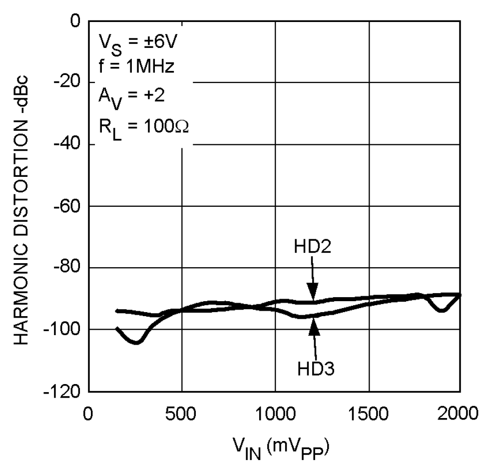
Harmonic Distortion vs. Input Signal Level



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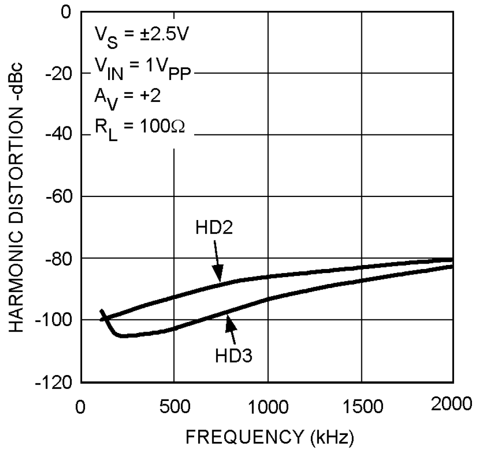
Typical Performance Characteristics (Continued)

Harmonic Distortion vs. Frequency



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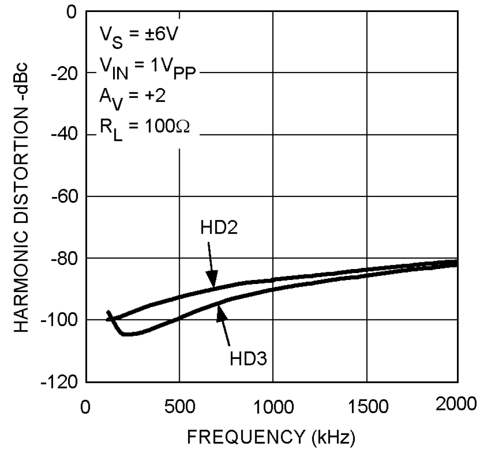
Harmonic Distortion vs. Frequency



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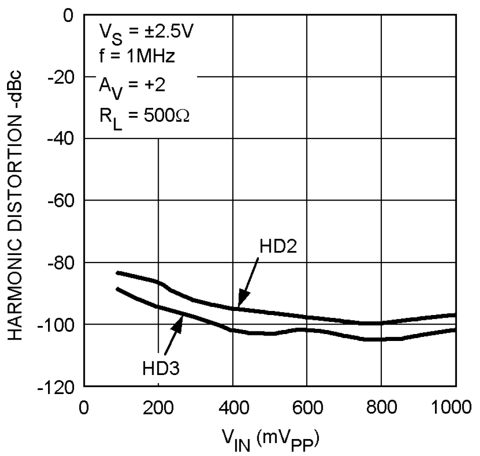
Harmonic Distortion vs. Input Signal Level



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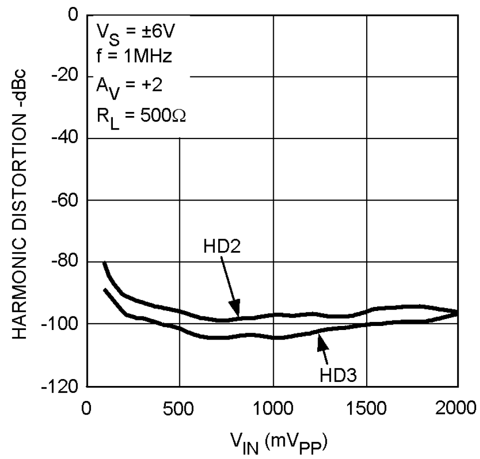
Harmonic Distortion vs. input Signal Level



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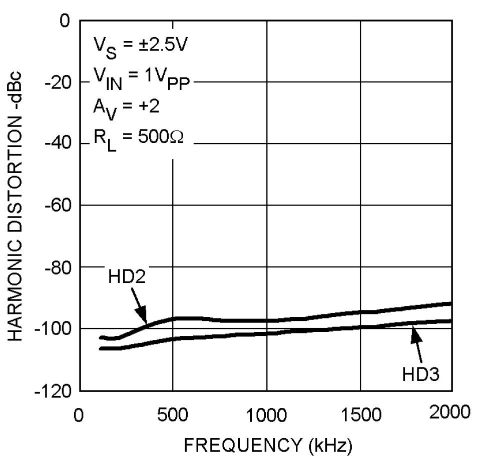
Harmonic Distortion vs. Input Frequency



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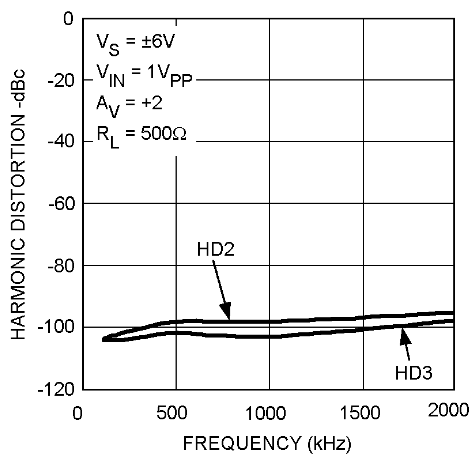
Harmonic Distortion vs. Input Frequency



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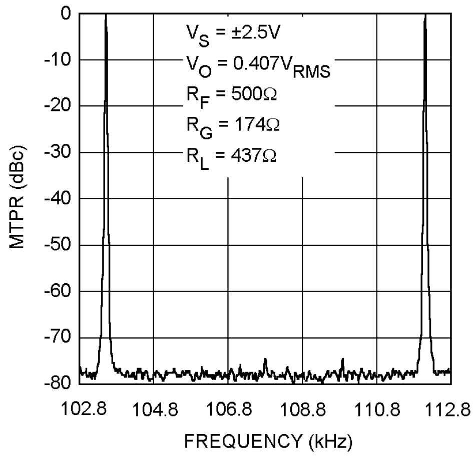
Typical Performance Characteristics (Continued)

Full Rate ADSL (DMT) Upstream MTPR @ V_S = ±2.5V



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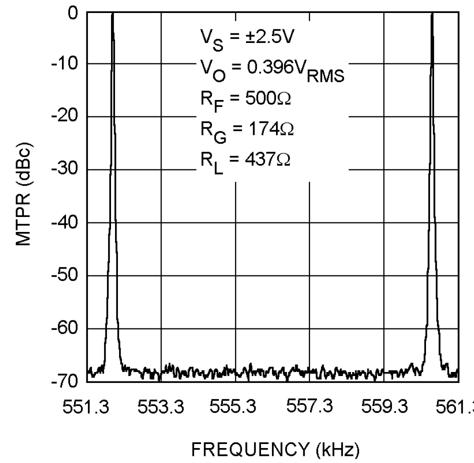
Full Rate ADSL (DMT) Downstream MTPR @ V_S = ±2.5V



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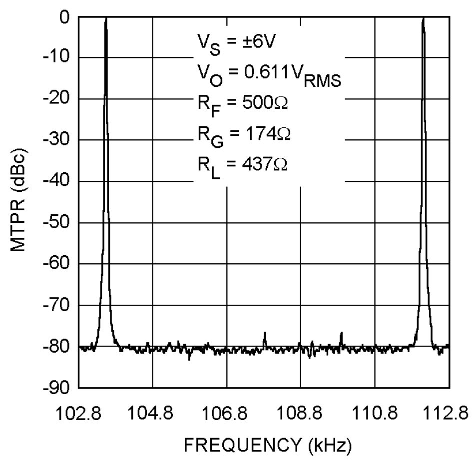
Full Rate ADSL (DMT) Upstream MTPR @ V_S = ±6V



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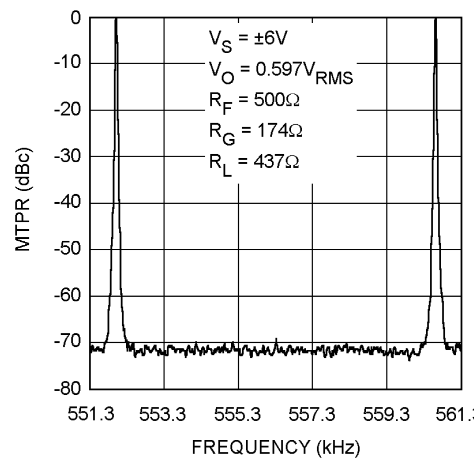
Full Rate ADSL (DMT) Downstream MTPR @ V_S = ±6V



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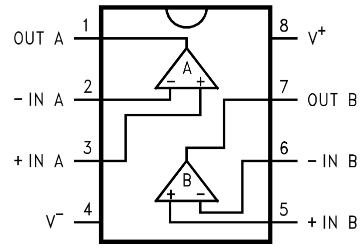
Connection Diagram

8-Pin SOIC/MSOP



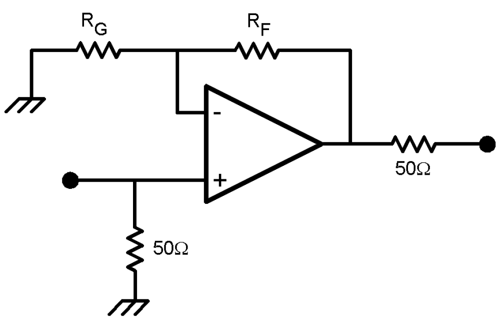
20029211

Top View

Ordering Information

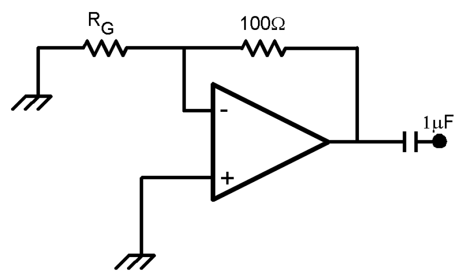
Package	Part Number	Package Marking	Transport Media	NSC Drawing
8-Pin SOIC	LMH6622MA	LMH6622MA	95 Units per Rail	M08A
	LMH6622MAX		2.5k Units Tape and Reel	
8-Pin MSOP	LMH6622MM	A80A	1k Units Tape and Reel	MUA08A
	LMH6622MMX		3.5k Units Tape and Reel	

Test Circuits



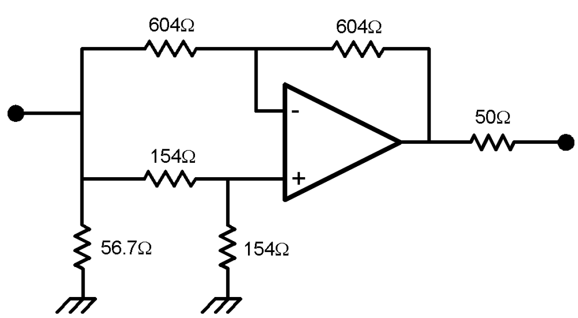
20029250

1) Non-Inverting Amplifier



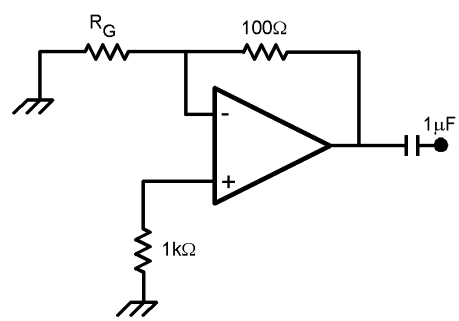
20029253

3) Voltage Noise
R_G = 1Ω for f ≤ 100kHz, R_G = 20Ω for f > 100kHz



20029251

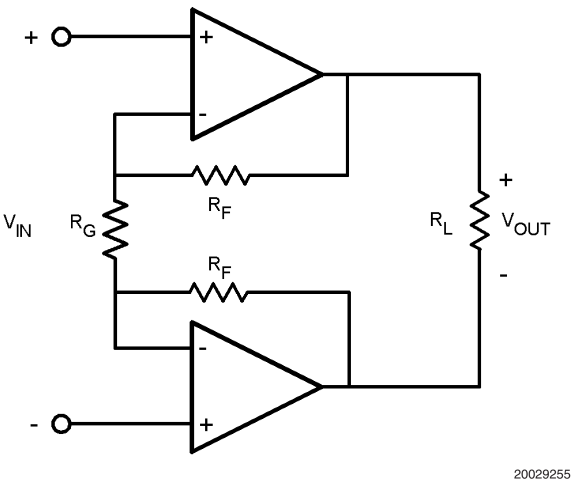
2) CMRR



20029252

4) Current Noise
R_G = 1Ω for f ≤ 100kHz, R_G = 20Ω for f > 100kHz

Test Circuits (Continued)



5) Multitone Power Ratio, R_F = 500Ω, R_G = 174Ω, R_L = 437Ω

DSL Receive Channel Applications

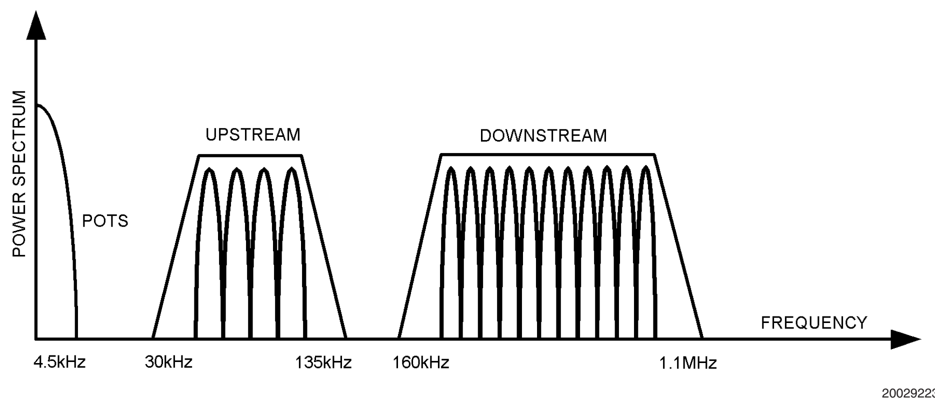


FIGURE 1. ADSL Signal Description

The LMH6622 is a dual, wideband operational amplifier designed for use as a DSL line receiver. In the receive band of a Customer Premises Equipment (CPE) ADSL modem it is possible that as many as 255 Discrete Multi-Tone (DMT) QAM signals will be present, each with its own carrier frequency, modulation, and signal level. The ADSL standard requires a line referred noise power density of -140dBm/Hz within the CPE receive band of 100KHz to 1.1MHz. The CPE driver output signal will leak into the receive path because of full duplex operation and the imperfections of the hybrid coupler circuit. The DSL analog front end must incorporate a receiver pre-amp which is both low noise and highly linear for ADSL-standard operation. The LMH6622 is designed for the twin performance parameters of low noise and high linearity.

Applications ranging from +5V to +12V or ±2.5V to ±6V are fully supported by the LMH6622. In *Figure 2*, the LMH6622 is used as an inverting summing amplifier to provide both received pre-amp channel gain and driver output signal cancellation, i.e., the function of a hybrid coupler.

DSL Receive Channel Applications (Continued)

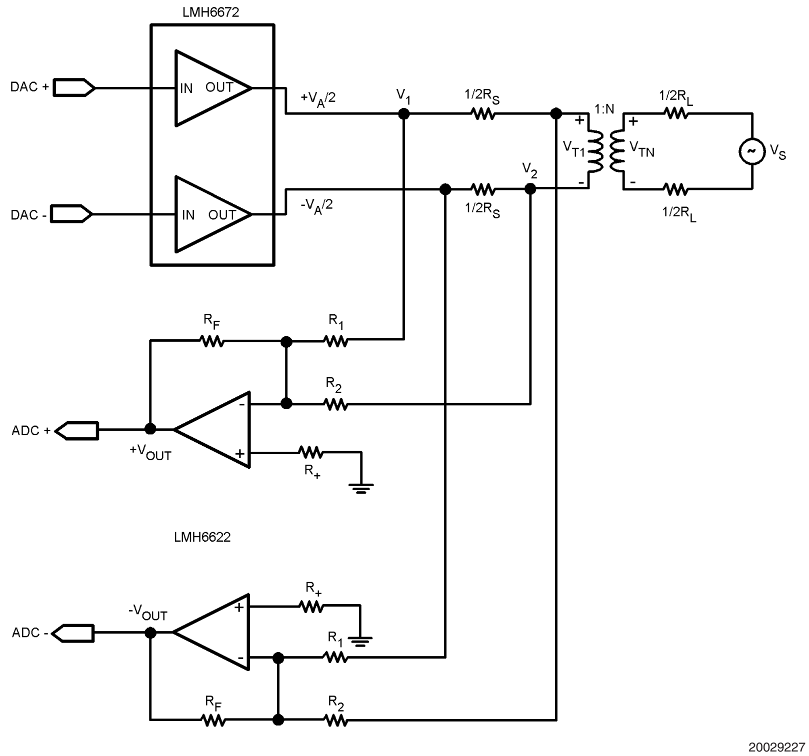


FIGURE 2. ADSL Receive Applications Circuit

DSL Receive Channel Applications

(Continued)

The two R_S resistors are used to provide impedance matching through the 1:N transformer.

$$R_S = \frac{R_L}{N^2}$$

Where R_L is the impedance of the twisted pair line.

N is the turns ratio of the transformer.

The resistors R_2 and R_F are used to set the receive gain of the pre-amp. The receive gain is selected to meet the ADC full-scale requirement of a DSL chipset.

Resistor R_1 and R_2 along with R_F are used to achieve cancellation of the output driver signal at the output of the receiver.

Since the LMH6622 is configured as an inverting summing amplifier, V_{OUT} is found to be,

$$V_{OUT} = -R_F\left[\frac{V_1}{R_1} + \frac{V_2}{R_2}\right]$$

The expression for V_1 and V_2 can be found by using superposition principle.

When $V_S = 0$,

$$V_1 = \frac{1}{2}V_A \quad \text{and} \quad V_2 = -\frac{1}{4}V_A$$

When $V_A = 0$,

$$V_1 = 0 \quad \text{and} \quad V_2 = -\frac{1}{2}V_{T1}$$

Therefore,

$$V_1 = \frac{1}{2}V_A \quad \text{and} \quad V_2 = -\frac{1}{4}V_A - \frac{1}{2}V_{T1}$$

And then,

$$V_{OUT} = -R_F\left[\frac{V_A}{2R_1} - \frac{V_A}{4R_2} - \frac{V_{T1}}{2R_2}\right]$$

Setting $R_1 = 2{*}R_2$ to cancel unwanted driver signal in the receive path, then we have

$$V_{OUT} = \frac{R_F}{2R_2}V_{T1}$$

We can also find that,

$$V_{TN} = \frac{1}{2}V_S \quad \text{and} \quad V_{T1} = \frac{1}{N}V_{TN} = \frac{1}{2N}V_S$$

And then

$$V_{OUT} = \frac{R_F}{4NR_2}V_S$$

In conclusion, the peak-to-peak voltage to the ADC would be,

$$2\ V_{OUT} = \frac{R_F}{2NR_2}V_S$$

RECEIVE CHANNEL NOISE CALCULATION

The circuit of *Figure 2* also has the characteristic that it cancels noise power from the drive channel.

The noise gain of the receive pre-amp is found to be:

$$A_N = 1 + \frac{R_F}{R_1 // R_2}$$

Noise power at each of the output of LMH6622:

$$e^2_o = A^2_n\,[V^2_n + i^2_{non\text{-}inv}\,R_+^{\,2} + 4kT\,R_+] + i^2_{inv}\,R^2_F + 4kT\,R_F\,A_n$$

where

V_n	Input referred voltage noise
i_n	Input referred current noise
$i_{non\text{-}inv}$	Input referred non-inverting current noise
i_{inv}	Input referred inverting current noise
k	Boltzmann's constant, K = 1.38 x 10^{-23}
T	Resistor temperature in k
R_+	Source resistance at the non-inverting input to balance offset voltage, typically very small for this inverting summing applications

For a voltage feedback amplifier,

$$i_{inv} = i_{non\text{-}inv} = i_n$$

Therefore, total output noise from the differential pre-amp is:

$$e^2_{TotalOutput} = 2\,e^2_o$$

The factor '2 ' appears here because of differential output.

DIFFERENTIAL ANALOG-TO-DIGITAL DRIVER

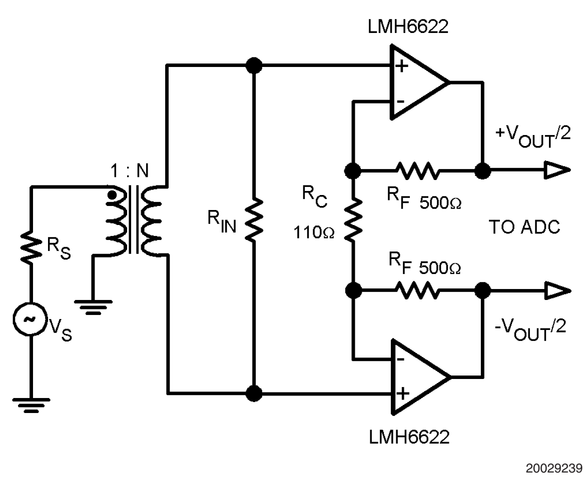


FIGURE 3. Circuit for Differential A/D Driver

DSL Receive Channel Applications

(Continued)

The LMH6622 is a low noise, low distortion high speed operational amplifier. The LMH6622 comes in either SOIC-8 or MSOP-8 packages. Because two channels are available in each package the LMH6622 can be used as a high dynamic range differential amplifier for the purpose of driving a high speed analog-to-digital converter. Driving a 1kΩ load, the differential amplifier of *Figure 3* provides 20dB gain, a flat frequency response up to 6MHz, and harmonic distortion that is lower than 80dBc. This circuit makes use of a transformer to convert a single-ended signal to a differential signal. The input resistor R_{IN} is chosen by the following equation,

$$R_{IN} = \frac{1}{N^2} R_S$$

The gain of this differential amplifier can be adjusted by R_C and R_F,

$$A_V = 2\frac{R_F}{R_C}$$

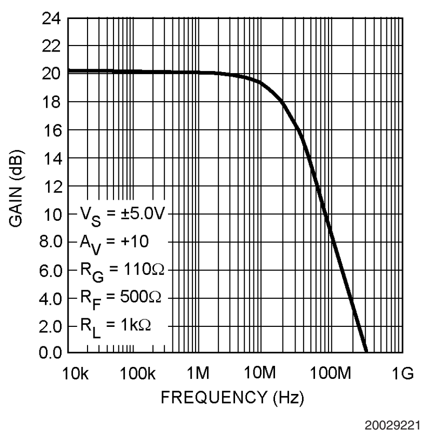


FIGURE 4. Frequency Response

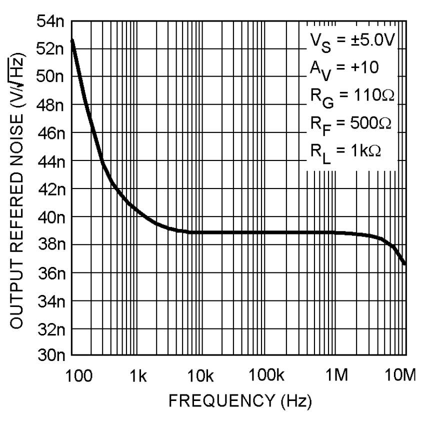


FIGURE 5. Total Output Referred Noise Density

CIRCUIT LAYOUT CONSIDERATIONS

National Semiconductor suggests the copper patterns on the evaluation boards listed below as a guide for high frequency layout. These boards are also useful as an aid in device testing and characterization. As is the case with all high-speed amplifiers, accepted-practice R_F design technique on the PCB layout is mandatory. Generally, a good high frequency layout exhibits a separation of power supply and ground traces from the inverting input and output pins. Parasitic capacitances between these nodes and ground will cause frequency response peaking and possible circuit oscillations (see Application Note OA-15 for more information). High quality chip capacitors with values in the range of 1000pF to 0.1µF should be used for power supply bypassing. One terminal of each chip capacitor is connected to the ground plane and the other terminal is connected to a point that is as close as possible to each supply pin as allowed by the manufacturer's design rules. In addition, a tantalum capacitor with a value between 4.7µF and 10µF should be connected in parallel with the chip capacitor. Signal lines connecting the feedback and gain resistors should be as short as possible to minimize inductance and microstrip line effect. Input and output termination resistors should be placed as close as possible to the input/output pins. Traces greater than 1 inch in length should be impedance matched to the corresponding load termination.

Symmetry between the positive and negative paths in the layout of differential circuitry should be maintained so as to minimize the imbalance of amplitude and phase of the differential signal.

Device	Package	Evaluation Board P/N
LMH6622MA	SOIC-8	CLC730036
LMH6622MM	MSOP-8	CLC730123

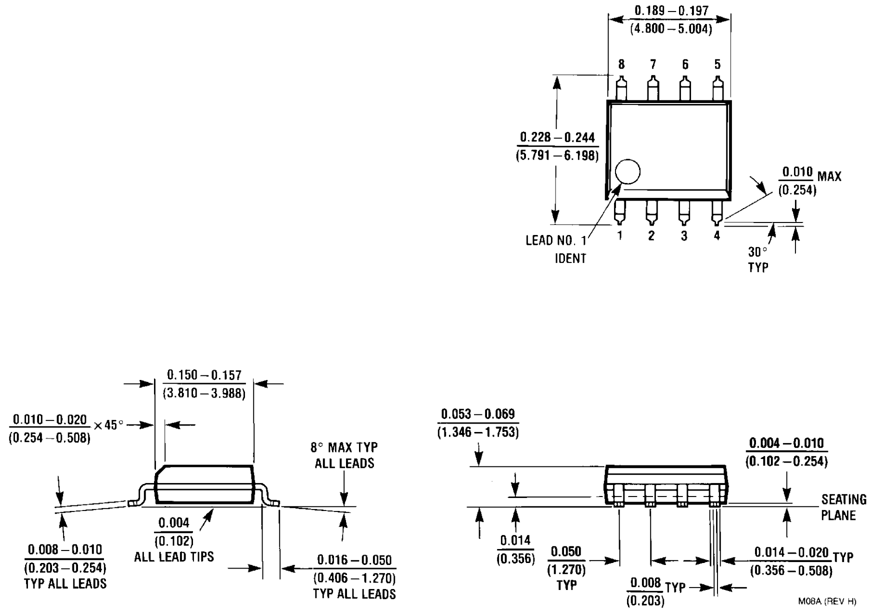
These free evaluation boards are shipped when a device sample request is placed with National Semiconductor.

Component value selection is another important parameter in working with high speed/high performance amplifiers. Choosing external resistors that are large in value compared to the value of other critical components will affect the closed loop behavior of the stage because of the interaction of these resistors with parasitic capacitances. These parasitic capacitors could either be inherent to the device or be a by-product of the board layout and component placement. Moreover, a large resistor will also add more thermal noise to the signal path. Either way, keeping the resistor values low will diminish this interaction. On the other hand, choosing very low value resistors could load down nodes and will contribute to higher overall power dissipation and worse distortion.

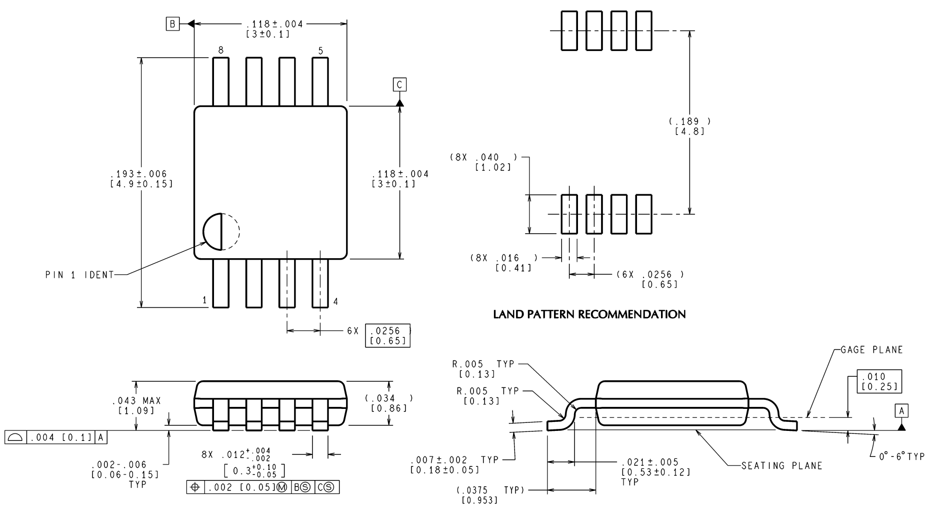
DRIVING CAPACITIVE LOAD

Capacitive Loads decrease the phase margin of all op amps. The output impedance of a feedback amplifier becomes inductive at high frequencies, creating a resonant circuit when the load is capacitive. This can lead to overshoot, ringing and oscillation. To eliminate oscillation or reduce ringing, an isolation resistor can be placed between the load and the output. In general, the bigger the isolation resistor, the more damped the pulse response becomes. For initial evaluation, a 50Ω isolation resistor is recommended.

Physical Dimensions inches (millimeters) unless otherwise noted



8-Pin SOIC
NS Package Number M08A



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MUA08A (Rev E)

8-Pin MSOP
NS Package Number MUA08A

Notes

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